Saeed Saeedi received the B.Sc., M.Sc. and Ph.D. degrees in electrical engineering from Sharif University of Technology, Tehran, Iran in 2001, 2003 and 2010, respectively. In 2012, he joined Tarbiat Modares University where he is now an assistant professor. His research interests include analog and RF integrated circuits for communication systems and high performance data converters.

Courses

Integrated Circuits for Optical Communications
MMIC Design
Data Converters
VLSI Design
RFIC Design
Linear IC Design

Research

Analog/RF and microwave integrated circuits
Design of communication transceivers
High speed/high resolution data converters

Students

Current MS Students:
-Behnam Abdollahi
-Elham Farahmand
-Poria Akbari
-Mojtaba Aghajan Nashtaee
-Mostafa Hasani
-Mahdi Derakhshan
-Soudabeh Fotouhi
-Baset Mesgari
-Samaneh Mousavi

Curriculum Vitae

Ph.D. Thesis: Wideband frequency synthesizer for digital video tuners
M.S. Thesis: A high speed 1.5-V digital to analog converter with a 14-bit self calibration technique

Journal papers

• M. Hasani and S. Saeedi, "Edge-combining multi-phase DLL frequency multiplier with reduced static phase offset and linearized delay transfer curve" Springer Analog Integrated Circuits and Signal Processing Journal, Vol.82, No.3, pp.705-718, March 2015.

• F. Akbar, M. Atarodi and S. Saeedi, "Design method for a reconfigurable CMOS LNA with input tuning and active balun," Elsevier International Journal of Electroics and Communications , Vol.69, No.1, pp.424-431, Jan 2015.

• S. Saeedi and M. Atarodi, "Single-VCO Multi-band DTV Frequency Synthesizer with a Divide-by-3 Frequency Divider for Quadrature Signal Generation," Springer Analog Integrated Circuits and Signal Processing Journal, Vol.64, No.2, pp.103-113, Aug. 2010.

• S. Saeedi and M. Atarodi, "Noise Canceling Balun-LNA with Enhanced IIP2 and IIP3 for Digital TV Applications," IEICE Transactions on Electronics, Vol. E95-C, No.1, Jan. 2012.

• S. Saeedi, S. Mehrmanesh and M. Atarodi, "A low voltage 14-bit self-calibrated CMOS DAC with enhanced dynamic linearity," Springer Analog Integrated Circuits and Signal Processing Journal, Vol.43, No.2, pp. 137-145, May 2005.

Conference papers

B. Mesgari, S. Saeedi and A. Jannesari, "A Wideband low noise distributed amplifier with active termination," IEEE International Symposium on Telecommunications (IST), 2014, pp.170-174.

• S. Saeedi, M. Atarodi and M. Sharif Bakhtiar, "A Divide-by-3 Frequency Divider for I/Q Generation in a Multi-band Frequency Synthesizer," IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS), 2008, pp.1383-1386.

• S. Saeedi, S. Mehrmanesh, A. Tajalli and M. Atarodi, "A Technique to Suppress Tail Current Flicker Noise in CMOS LC VCOs," IEEE International Symposium on Circuits and Systems (ISCAS), 2006, pp. 3229-3232.

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CMOS DAC with enhanced dynamic linearity," IEEE International Symposium on Circuits and Systems (ISCAS), 2004, Vol. I, pp. 349-352.

• S Saeedi, S. Mehrmanesh, M. Atarodi and H. A. Aslanzadeh, "A 1.5-V 14-Bit CMOS DAC with a new Self-Calibration Technique for Wireless Communication Systems," IEEE International Conference on Electronics Circuits and Systems (ICECS), 2003, pp. 786-789.

• F. Aghlmand, M. Atarodi and S. Saeedi, "Low Phase Noise On-Chip Oscillator for Implantable Biomedical Applications," IEEE International Symposium on Circuits and Systems (ISCAS), 2011, pp. 213-216.

• M. Gholami, M. Sharifkhani, S. Saeedi, "Modeling of DLL-based frequency multiplier in time and frequency domain with Matlab Simulink", IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS), 2010, pp.1051-1054.

• M. Gholami, M. Sharifkhani, A. Ebrahimi, S. Saeedi, M. Atarodi, "Systematic modeling and simulation of DLL-based frequency multiplier," International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD), 2010.

• M. Gholami, M. Sharifkhani, S. Saeedi, M. Atarodi, "A DLL-based frequency synthesizer for VHF DVB-H/T receivers", International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD), 2010.

• S. Mehrmanesh, B. Eghbalkhah, S. Saeedi, A. Afzali-Kusha and M. Atarodi, " A compact low power mixed-signal equalizer for gigabit ethernet applications," IEEE International Symposium on Circuits and Systems (ISCAS), 2006, pp. 5167-5170.

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